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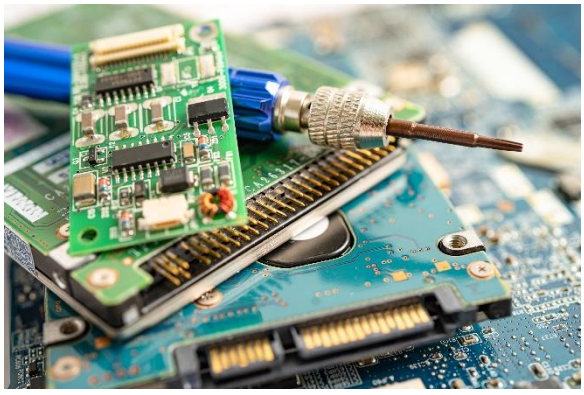
TECH OFFER

PARALLEL SELF TIMED FAST ADDER



MORE INFORMATION

MEGA-TREND

- Electronics and Security

TECHNOLOGY READINESS LEVEL (TRL)

- TRL 3

PATENT/ GRANTED NUMBER

- MY-177563-A

TECHNOLOGY OVERVIEW

A parallel self-timed adder (pasta) is disclosed. It is based on recursive formulation and uses only half adders for performing multi-bit binary addition. Theoretically the operation is parallel for those bits that do not need any carry chain propagation. Thus the new approach attains logarithmic performance without any special speed-up circuitry or look-ahead schema. The corresponding CMOS implementation of the design along with completion detection unit is also presented. The design is regular and does not have any practical limitations of fan-ins or fan-outs or complex interconnections.

Thus it is more suitable for adoption in fast adder implementation in high-performance processors. The performance of the implementation is tested using spice circuit simulation tool by linear technology. Simulation results show its superiority over cascaded circuit adders. A constant time carry propagation is also achieved using the proposed implementation by tuning the CMOS parameters.

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